REMARKS

Claims 1-3, 7-11, and 15 are currently pending in this action while claims 4-6, 12-14, and 16-20 had been previously withdrawn. Claims 1-2 and 7-9 stand rejected under 35 USC §102(e) as being anticipated by Barns, et al. (US Patent No. 6,743,683). Claims 1-3, 7-10, 11, and 15 stand provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 10/739,173 and 10/742,678. Applicants have amended claims 1 and 2. In view of the amendments and arguments set forth below, Applicants respectfully submit that all pending claims are now in condition for allowance.

REJECTION OF CLAIMS 1-2 and 7-9 UNDER 35 USC §102(e)

The Examiner has rejected claims 1-2 and 7-9 under 35 USC §102(e) as being anticipated by Barns. The Applicants respectfully traverse the Examiner's rejections.

According to MPEP 706.02, "for anticipation under 35 USC 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present." Applicant respectfully submits that in the present application, Barnes does not expressly or impliedly teach all of the elements recited in amended claim 1. More specifically, Barnes does not teach using the etch stop layer to prevent the formation of a silicide layer on the sacrificial gate electrode, as explained below.

Barns and claim 1 both teach methods of forming a metal gate electrode by way of a replacement gate process. Both methods also teach forming silicide layers on the source and drain regions of the transistors. One significant difference, however, is that the process taught by Barnes includes the formation of a silicide layer on the sacrificial gate electrode (see Figure 9 of Barnes, as well as col. 2, lines 24-31). This silicide layer is generally difficult to remove. For instance, if a CMP process is used, the CMP slurry must be capable of simultaneously removing a dielectric layer, a silicon nitride layer, and a silicide

layer (see Barnes, col. 3, lines 3-20). The formation of silicide therefore adversely impacts the removal of the sacrificial gate electrode.

Contrary to Barns, the Applicants' claim 1 teaches an improved process that does not allow a silicide layer to be formed on the sacrificial gate electrode. As recited in amended claim 1, when the silicide layers are formed near the first and second spacers, "*the etch stop layer inhibits the formation of a silicide layer on any portion of the sacrificial gate electrode layer....*" The process flow provided in claim 1 therefore enables silicide layers to be formed on the source and drain regions of the transistor without adversely impacting the subsequent removal of the sacrificial gate electrode. The CMP slurry used to expose the sacrificial gate electrode only has to be capable of removing a dielectric layer and a silicon nitride layer. The CMP process does not have to remove a silicide layer, which makes the CMP process less complex and generally less costly.

Support for the amendments made to claim 1 can be found at paragraphs 0005 and 0018 of the Applicants' specification.

Because Barnes does not teach or suggest a process that prevents a silicide layer from being formed on the sacrificial gate electrode, it cannot be used to support a 35 USC 102(e) rejection of claim 1. Therefore, the Applicants believe the 102(e) rejection of independent claim 1, as well as dependent claims 2 and 7-9, cannot stand, and allowance of these claims is respectfully requested.

PROVISIONAL REJECTION OF CLAIMS 1-3, 7-10, 11, and 15

Claims 1-3, 7-10, 11, and 15 stand provisionally rejected on the ground of nonstatutory obviousness-type double patenting. The Applicants have executed and attached Two terminal disclaimers. As such, the Applicants' believe the Examiner's provisional rejection has been overcome.

CONCLUSION

Applicant submits that all claims now pending are in condition for allowance. Applicant reserves the right to argue the patentability of the dependent claims. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Account No. 02-2666.

Respectfully submitted,

Date: March 14, 2006

/Rahul D. Engineer/
Rahul D. Engineer
Reg. No. 47,548